Z87000/Z87L00

Spread Spectrum Controllers

Customer Procurement Specification

DS96WRL0501

ZiLOG Worldwide Headquarters • 910 E. Hamilton Avenue • Campbell, CA 95008
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

PRELIMINARY

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
910 E. Hamilton Avenue
Campbell, CA 95008
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

Z87000/Z87L00

SPREAD SPECTRUM CONTROLLERS

FEATURES

Device	ROM (KWords)	RAM* (Words)	I/O Lines	Package Information
Z87000	12	512	32	84-Pin PLCC 100-Pin QFP
Z87L00	12	512	32	100-Pin QFP

Note: *General-Purpose

- Transceiver/Controller Chip Optimized for Implementation of 900 MHz Spread Spectrum Cordless Phone
  - Adaptive Frequency Hopping
  - Transmit Power Control
  - Error Control Signaling
  - Handset Power Management
  - Support of 32 kbps ADPCM Speech Coding for High Voice Quality
- DSP Core Acts as Phone Controller
  - Zilog-Provided Embedded Transceiver Software to Control Transceiver Operation and Base Station-Handset Communications Protocol
  - User-Modifiable Software Governs Phone Features
- Transceiver Circuitry Provides Primary Cordless Phone Communications Functions
  - Digital Downconversion with Automatic Frequency Control (AFC) Loop
  - FSK Demodulator
  - FSK Modulator
  - Symbol Synchronizer
  - Time Division Duplex (TDD) Transmit and Receive Buffers
- On-Chip A/D and D/A to Support 10.7 MHz IF Interface
- Bus Interface to Z87010 ADPCM Processor
- Static CMOS for Low Power Consumption
- 3.0V to 3.6V, -20°C to +70°C, Z87L00
  4.5V to 5.5V, -20°C to +70°C, Z87000
- 16.384 MHz Base Clock

GENERAL DESCRIPTION

The Z87000/Z87L00 FHSS Cordless Telephone Transceiver/Controllers are expressly designed to implement a 900 MHz frequency hopping spread spectrum cordless telephone compliant with United States FCC regulations for unlicensed operation. The Z87000 and Z87L00 are distinct 5V and 3.3V versions, respectively, of the device. For the sake of brevity, all subsequent references to the Z87000 in this document also apply to the Z87L00, unless specifically noted.

The Z87000 supports a specific cordless phone system design that uses frequency hopping and digital modulation to provide extended range, high voice quality, and low system costs.The Z87000 uses a Zilog 16-bit fixed-point two's complement static CMOS Digital Signal Processor core as the phone and RF section controller. The Z87000's DSP core processor further supports control of the RF section's frequency synthesizer for frequency hopping and the generation of the control messages needed to coordinate incorporation of the phone's handset and base station.

GENERAL DESCRIPTION (Continued)

Additional on-chip transceiver circuitry supports Frequency Shift Keying modulation/demodulation and multiplexing/demultiplexing of the 32 kbps voice data and 4 kbps command data between handset and base station. The Z87000 provides thirty-two I/O pins, including four wake-up inputs and two CPU interrupt inputs. These programmable I/O pins allow a variety of user-determined phone features and board layout configurations. Additionally, the pins may be used so that phone features and interfaces are supported by an optional microcontroller rather than by the Z87000's DSP core.

In combination with an RF section designed according to the system specifications, Zilog's Z87010/Z87L10 ADPCM Processor, a standard 8-bit PCM telephone CODEC and minimal additional phone circuity, the Z87000 and its embedded software provide a total system solution.

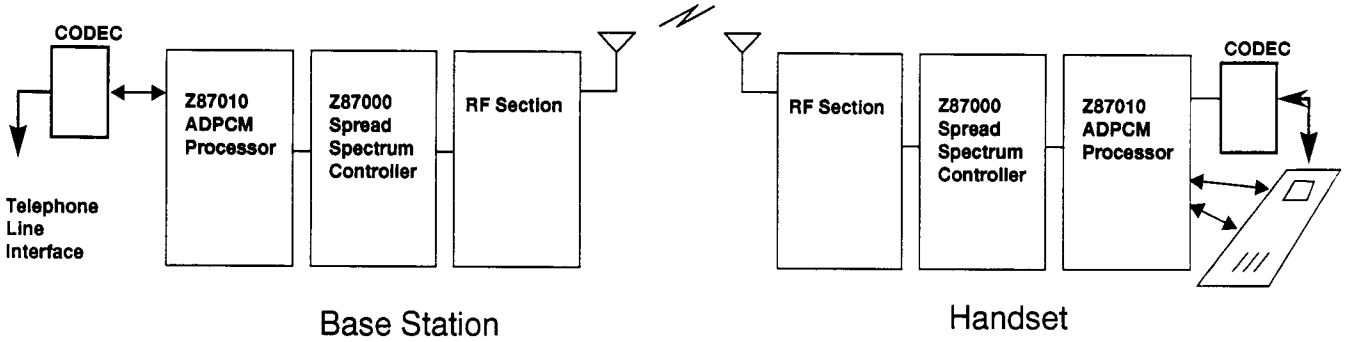


Figure 1. System Block Diagram of a Z87000/Z87010 Based Phone

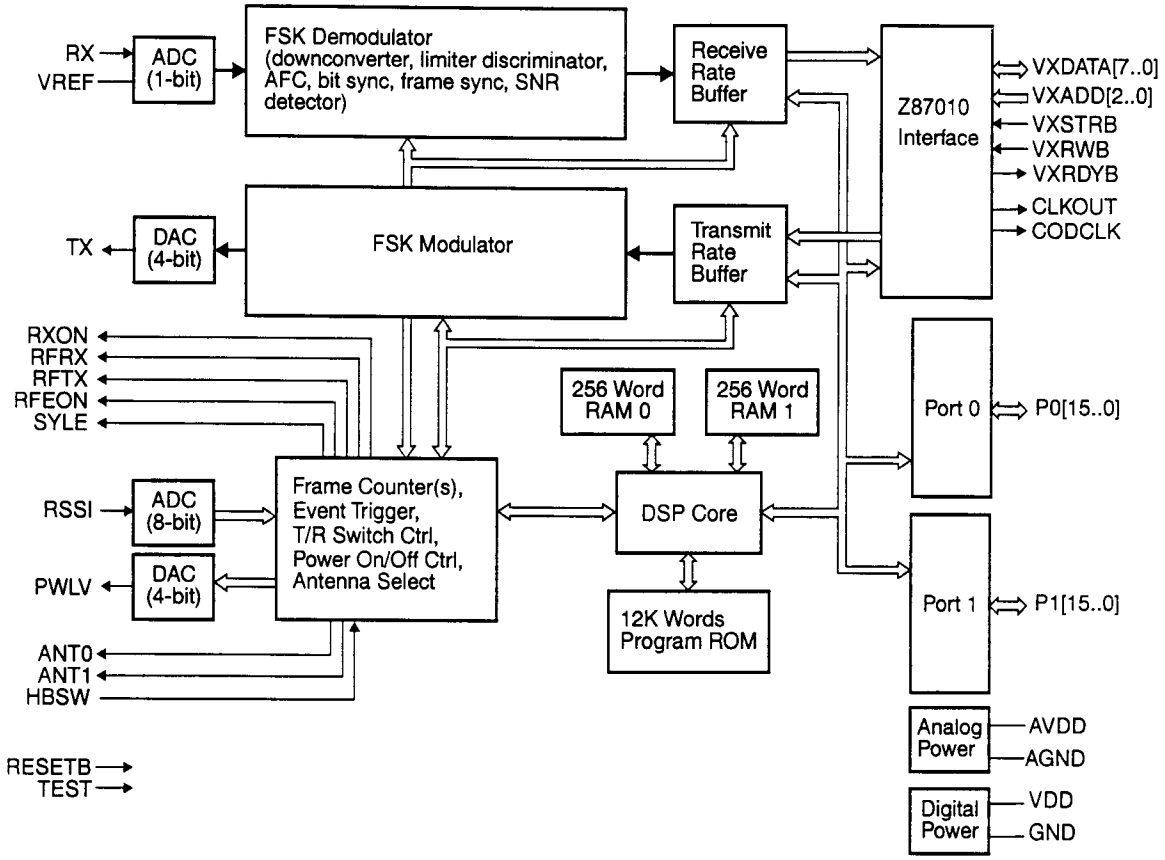


Figure 2. Z87000 Functional Block Diagram

PIN DESCRIPTION

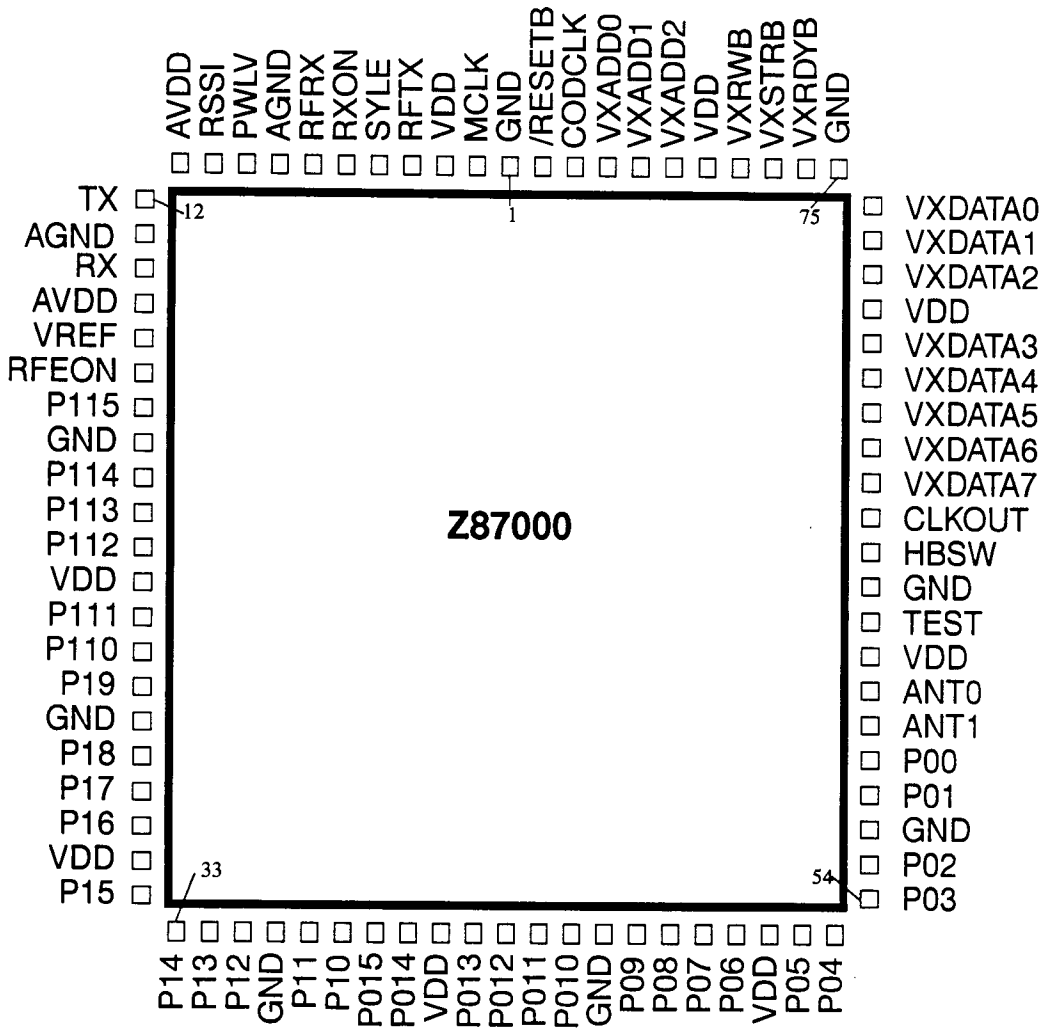


Figure 3. 84-Pin PLCC ROM Pin Configuration (Z87000 only)

Table 1. 84-Pin PLCC Pin Description Summary

Pin Number	Symbol	Function	Direction
1,19,27,36,46, 56,63,75	GND	Ground	–
2	MCLK	Master clock (16.384 MHz)	Input
3,23,31,41,51, 61,71,79	V_{DD}	Digital	–
4	RFTX	RF transmit switch control	Output
5	SYLE	RF synthesizer load enable	Output
6	RXON	Demodulator "on" indication	Output
7	RFRX	RF receive switch control	Output
8,13	AGND	Analog ground	–
9	PWLV	RF transmit power level	Output
10	RSSI	RF receive signals strength indicator	Input
11,15	AV_{DD}	Analog V_{DD}	–
12	TX	Analog transmit IF signal	Output
14	RX	Analog receive IF signal	Input
16	V_{REF}	Analog reference voltage for RX signal	Output
17	RFEON	RF module on/off control	Output
18,20,21,22,24, 25,26,28,29,30, 32,33,34,35,37,38	P115	General-purpose	Input
59,60	ANT1	RF diversity antenna control	Input/Output
62	TEST	Main test mode control	Input
64	HBSW	Handset/Base Control	–
65	CLKOUT	Clock output to ADPCM Processor	Output
76	VXRDYB	ADPCM processor ready signal	Output
77	VXSTRB	ADPCM processor data strobe	Input
78	VXRWB	ADPCM read/write control	Input
80,81,82	VXADD2	ADPCM processor address bus	Input
83	CODCLK	Clock output to codec	Output
84	/RESETB	Reset signal	Input

PIN DESCRIPTION (Continued)

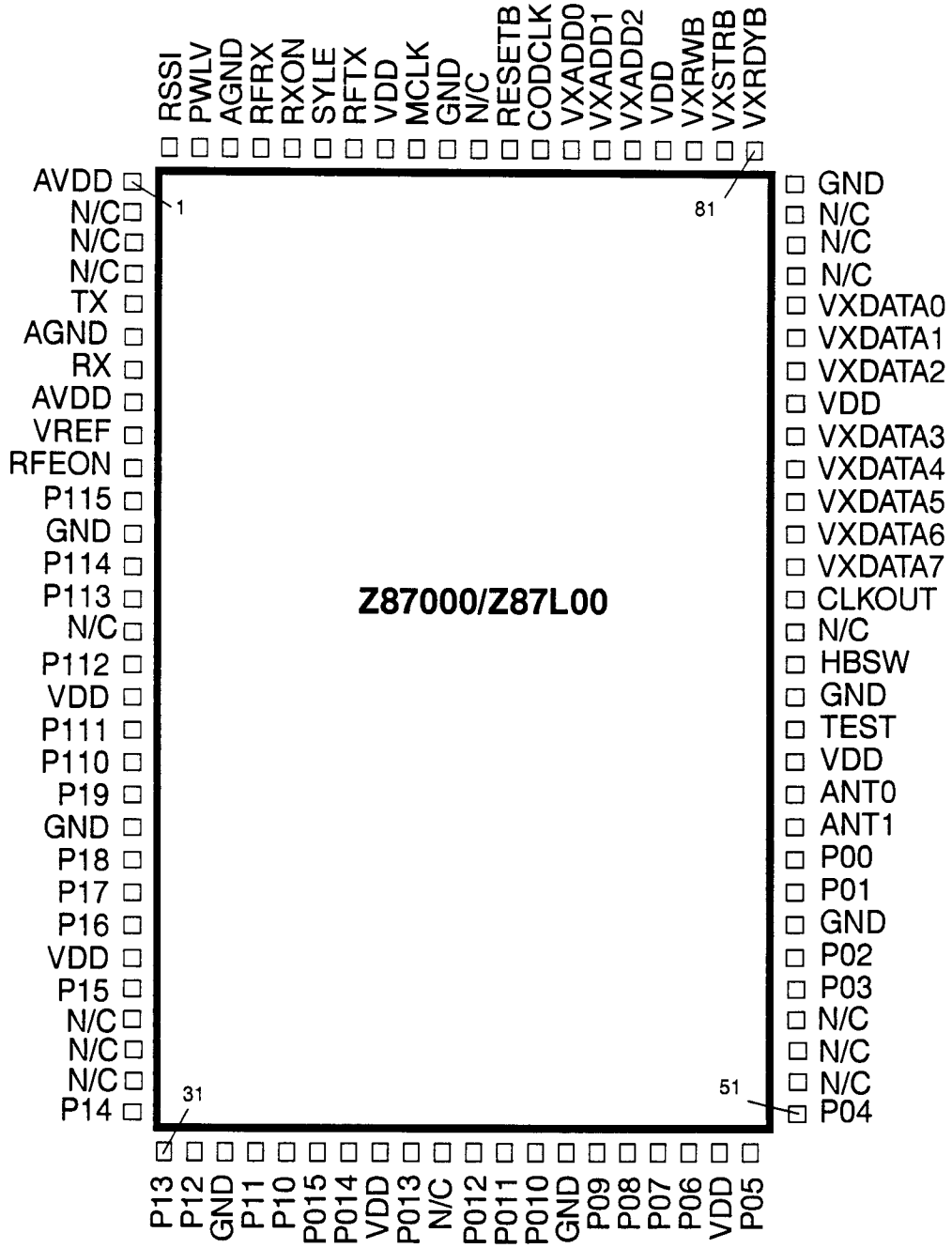


Figure 4. 100-Pin QFP Pin Configuration

Table 2. 100-Pin QFP Pin Configuration

No	Symbol	Function	Direction
1,8	AV_{DD}	Analog V_{DD}	–
2,3,4,15,27,28, 29,40,52,53,54, 66,77,78,79,90	N/C	No connection	–
5	TX	Analog transmit IF signal	Output
6,98	AGND	Analog ground	–
7	RX	Analog receive IF signal	Input
9	VREF	Analog reference voltage for RX signal	–
10	RFEON	RF module on/off control	Output
11,13,14,16,18, 19,20,22,23,23, 26,30,31,32,34,35	P1[15..0]	General-purpose I/O port 0	Input
17,25,38,49,62, 73,84,93	V_{DD}	Digital	–
36,37,39,41,42, 43,45,46,47,48, 50,51,55,56,58,59	P0[15..0]	General-purpose I/O port 0	Input
60,61	ANT[1..0]	RF diversity antenna control	Input/Output
63	TEST	Main test mode control	Input
65	HBSW	Handset/bast control	Input
67	CLKOUT	Clock output to ADPCM processor	Output
68,69,70,71,72, 74,75,76	VXDATA[7..]	ADPCM processor data bus	Input
81	VXRDYB	ADPCM processor ready signal	Output
82	VXSTRB	ADPCM processor data strobe	Input
83	VXRWB	ADPCM processor read/write control	Input
85,86,87	VXADD[2..0]	ADPCM processor address bus	Input
88	CODCLK	Clock output to codec	Output
89	/RESETB	Reset signal	Input
92	MCLK	Master clock input (16.384 MHz)	Input
94	RFTX	RF transmit switch control	Output
95	SYLE	RF synthesizer load enable	Output
96	RXON	Demodulator "on" indication	Output
97	RFRX	RF receive switch control	Output
99	PWLV	RF transmit power level	Input
100	RSSI	RF receive signal strength indicator	Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	DC Supply Voltage(1)	-0.5	7.0	V
V_{IN}	Input Voltage(2)	-0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage(3)	-0.5	V_{DD} + 0.5	V
T_A	Operating Temperature	-20	+70	°C
T_{STG}	Storage Temperature	-65	+150	°C

Notes:

1. Voltage on all pins with respect to GND.
2. Voltage on all inputs WRT VDD
3. Voltage on all outputs WRT VDD

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The electrical characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pins. Standard test conditions are as follows:

- $3.0V < V_{DD} < 3.6V$ (Z87L00)
- $4.5V < V_{DD} < 5.5V$ (Z87000)
- GND = 0V
- T_A = -20 to +70 °C

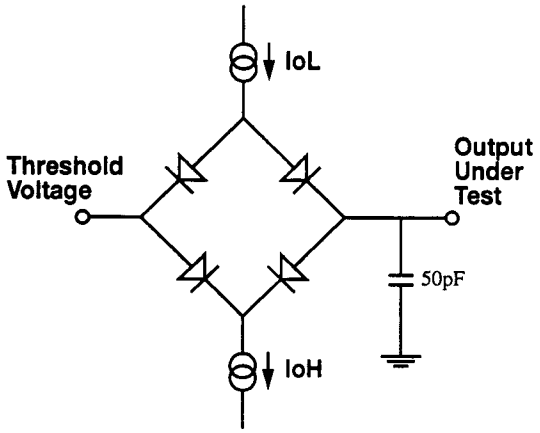


Figure 5. Test Load Diagram

RECOMMENDED OPERATING CONDITIONS

Table 3. 5V ± 0.5V Operation (Z87000)

Symbol	Parameter	Min	Max	Units
V_{DD}, AV_{DD}	Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.0	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.8	V
I_{OH}	Output High Current		-2.0	mA
I_{OL1}	Output Low Current		4.0	mA
I_{OL2}	Output Low Current, Ports (limited usage, 1)		12.0	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]

Table 4. 3.3V ± 0.3V Operation (Z87L00)

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	3.0	3.6	V
V_{IH}	Input High Voltage	0.7 V_{DD}	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	GND -0.3	0.1 V_{DD}	V
I_{OH}	Output High Current		-1.0	mA
I_{OL1}	Output Low Current		2.0	mA
I_{OL2}	Output Low Current, Ports (limited usage, 2)		6.0	mA
T_A	Operating Temperature	-20	+70	°C

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]

DC ELECTRICAL CHARACTERISTICS

Conditions for DC characteristics are corresponding operating conditions, and standard test conditions, unless otherwise specified.

Table 5. 5V ± 0.5V Operation (Z87000)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	2.4		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.6	V
V_{OL2}	Output Low Voltage, Ports (1)	V_{DD} min, I_{OL2} max		1.2	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			80	mA
I_{CC2}	Standby Mode Current (2)			4	mA

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]
2. 2.3 mA typical at 25°C, 5 volts.

Table 6. 3.3V ± 0.3V Operation (Z87L00)

Symbol	Parameter	Test Condition	Min	Max	Units
V_{OH}	Output High Voltage	V_{DD} min, I_{OH} max	1.6		V
V_{OL1}	Output Low Voltage	V_{DD} min, I_{OL1} max		0.4	V
V_{OL2}	Output Low Voltage, Ports(1)	V_{DD} min, I_{OL2} max		1.2	V
I_L	Input Leakage	V_{IN} = 0V, V_{DD}	-2	2	µA
I_{CC}	Supply Current			55	mA
I_{CC2}	Standby Mode Current(2)		1.4		mA

Notes:
1. Maximum 3 pins total from P0[15..0] and P1[15..0]
2. 1.6 mA typical at 25°C, 3.3 volts.

ANALOG CHARACTERISTICS

Table 7. 1-Bit ADC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	1	-	bit
Power dissipation	0.54 (70°c)	1.0 (40°c)	2.75 (-20°c)	mW
Power dissipation, Stop mode	0.06 (70°c)	0.2 (40°c)	1.1 (-20°c)	mW
Sample frequency	-	8.192	-	MHz
Sample window(1)	29	31	33	ns
Bandwidth	-	60	-	MHz
Supply Range(=AV_{DD})				
Z87L00	3.0		3.6	V
Z87000	4.5		5.5	V
Acquisition time	2	3	8	ns
Settling time	8	10	18	ns
Conversion time	4	6	18	ns
Aperture delay	2	3	8.5	ns
Aperture uncertainty(2)	-	-	0.5	ns
Input voltage range (p-p)	800	1000	1200	mV
Reference voltage				
Z87L00	1.7 (AV_{DD}= 3V)	1.9 (AV_{DD}= 3.3V)	2.1 (AV_{DD}= 3.6V)	V
Z87000	2.7 (AV_{DD}=4.5V)	3.0 (AV_{DD}= 5V)	3.3 (AV_{DD}= 5.5V)	V
Input resistance	10	18	25	KOhm
Input capacitance	-	10	-	pF

Notes:
Window of time while input signal is applied to sampling capacitor; see next figure.
Uncertainty in sampling time due to random variations such as thermal noise.

ANALOG CHARACTERISTICS (Continued)

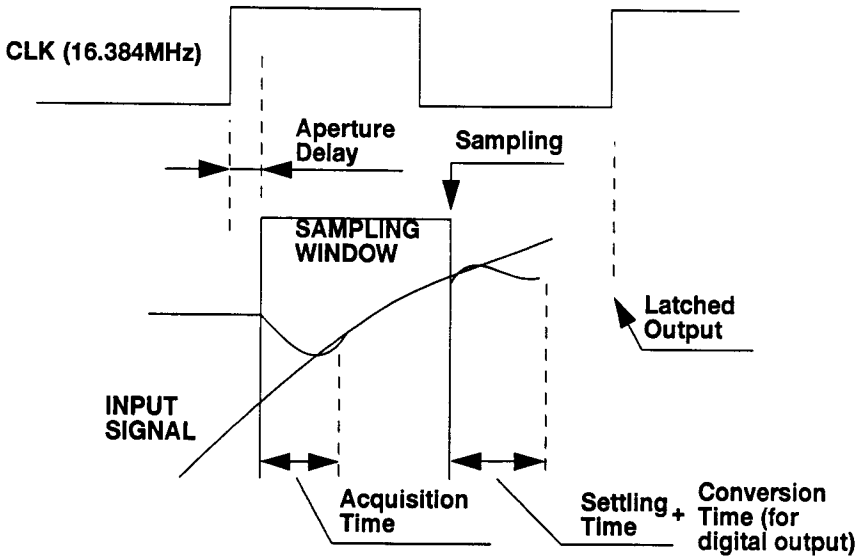


Figure 6. 1-Bit ADC Definition of Terms

Table 8. 8-bit ADC (Temperature -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	6	-	bit
Integral non-linearity	-	0.5	1	LSB
Differential non-linearity	-	-	0.5	LSB
Power Dissipation (peak)		35	70	mW
Sample window	5	-	120	ns
Bandwidth	-	-	2	Msps
Supply Range (=AV_{DD})				
Z87L00	3.0	3.3	3.6	V
Z87000	4.5	5.0	5.5	V
Input voltage range		0-AV_{DD}		V
Conversion time	0.5	-	-	µs
Aperture delay	2	3	8.5	ns
Aperture uncertainty	-	-	1	ns
Input resistance	-	25	-	Kohm
Input capacitance	-	10	-	pF

Notes:
1. 8-bit ADC only tested for 6-bit resolution.

Table 9. 4-bit DAC (Temperature: -20/+70°C)

Parameter	Minimum	Typical	Maximum	Units
Resolution	-	4	-	bit
Integral non-linearity	-	0.25	0.5	LSB
Differential non-linearity	-	0.25	1	LSB
Settling time (1/2 LSB)	-	-	22.5	ns
Zero error at 25°C	-	1	2	mV
Conversion time (input change to output change)	14	19	76	ns
Power dissipation, 25 pF load	1.2 (70°c)	20 (40°c)	24.1 (-20°c)	mW
Power dissipation, 25 pF load, Stop mode	0.18 (70°c)	1.0 (40°c)	1.1 (-20°c)	mW
Conversion time (input change to output change)	14.5	19.1	75.8	ns
Rise time (full swing)	11	15	71	ns
Output slew rate	8	67	96	V/µs
Output voltage range	-	0.2 AV_{DD} to 0.6AV_{DD}	-	V
Supply Range (=AV_{DD})				
Z87L00	3.0	3.3	3.6	V
Z87000	4.5	5.0	5.5	V
Output load resistance		330		Ohm
Output load capacitance	-	25	-	pF

INPUT/OUTPUT PIN CHARACTERISTICS

All digital pins (all pins except V_{DD}, AV_{DD}, GND, AGND, V_{REF}, RX, TX, RSSI and PWLV) have an internal capacitance of 5 pF.

The RX analog input pin has an input capacitance of 10 pF.

The RSSI analog input pin has an input capacitance of 10 pF.

AC ELECTRICAL CHARACTERISTICS

Clocks, Reset and RF Interface

Table 10. Clocks, Reset and RF Interface

No.	Symbol	Parameter	Min	Max	Units
1	TpC	MCLK input clock period (1)	61	61	ns
2	TwC	MCLK input clock pulse width	20	40	ns
3	TrC, TfC	MCLK input clock rise/fall time		15	ns
4	TrCC, TfCC	CLKOUT output clock rise/fall time	2	6	ns
5	TrCO, TfCO	CODCLK output clock rise/fall time	2	6	ns
6	TwR	RESETB input low width	18		TpC
7	TrRF, TfRF	RF output controls rise/fall time (2)	2	6	ns

Notes:
1. MCLK is 16.384 MHz ± 25 ppm
2. RF Controls are RFTX, RFRX, RXON, RFEON, SYLE.

ADPCM Processor Interface

The Z87000 is a peripheral device for the ADPCM Processor. The interface from the Z87000 perspective is composed of an input address bus, a bidirectional data bus, strobe and read/write input control signals and a ready/wait output control signal.

READ CYCLES refer to data transfers from the Z87000 to the ADPCM Processor.

WRITE CYCLES refer to data transfers from the ADPCM Processor to the Z87000.

Table 11. Read Cycles

Signal Name	Function	Direction
VXADD[2..0]	Address Bus	ADPCM Proc. to Z87000
VXDATA[7..0]	Data Bus	Bidirectional
VXSTRB	Strobe Control Signal	ADPCM Proc. to Z87000
VXRWB	Read/Write Control Signal	ADPCM Proc. to Z87000
VXRDYB	Ready Control Signal	Z87000 to ADPCM Proc.

Table 12. Write Cycles

No.	Symbol	Parameter	Min	Max	Units
8	TsAS	Address, Read/Write setup time before Strobe falls	10		ns
9	ThSA	Address, Read/Write hold time after Strobe rises	3		ns
10	TaDrS	Data read access time after Strobe falls		30 (1)	ns
11	ThDrS	Data read hold time after Strobe rises	8.5	40 (2)	ns
12	TwS	Strobe pulse width	20		
13	TsDwS	Data write setup time before Strobe rises	10		ns
14	ThDwS	Data write hold time after Strobe rises	3		ns
15	TaDrRY	Data read valid before Ready falls	22		ns
16	TdSRY	Strobe high after Ready falls	0		ns

Notes:
1. Requires wait state on ADPCM Processor read cycles
2. Requires no write cycle directly following read cycle on ADPCM Processor

AC TIMING DIAGRAMS

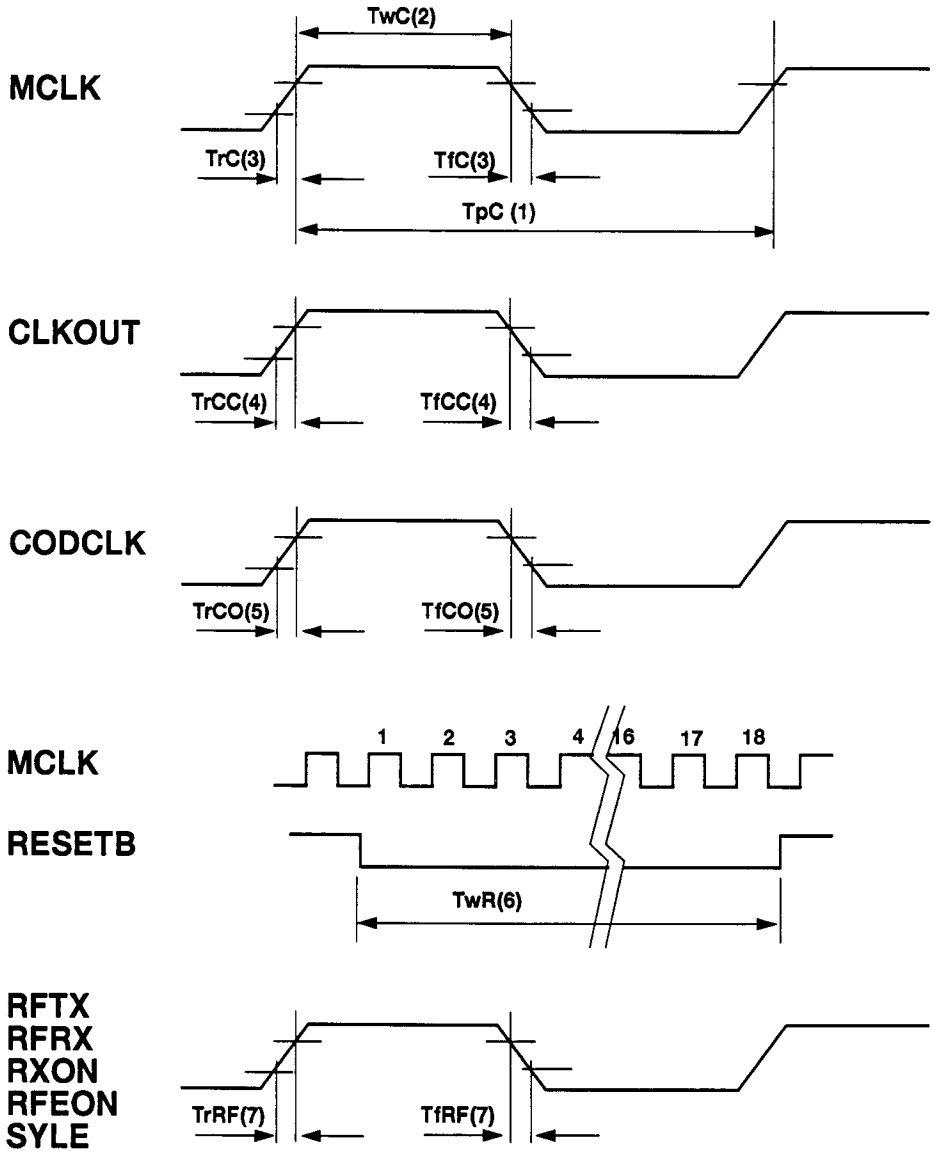
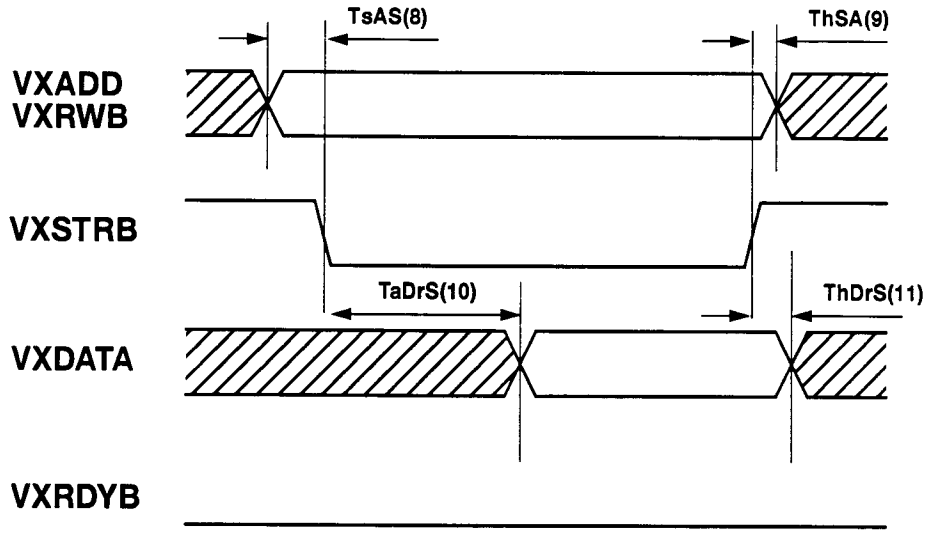
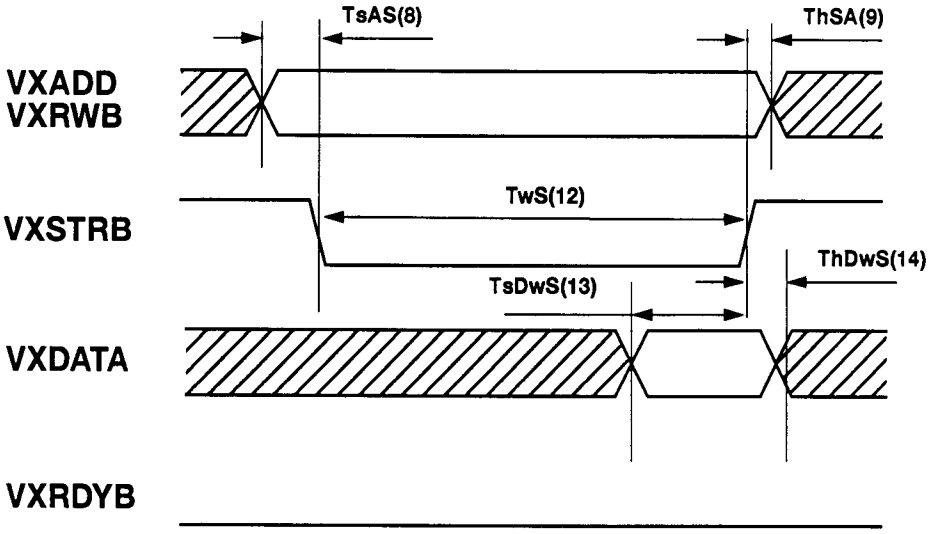


Figure 7. Transceiver Output Signal



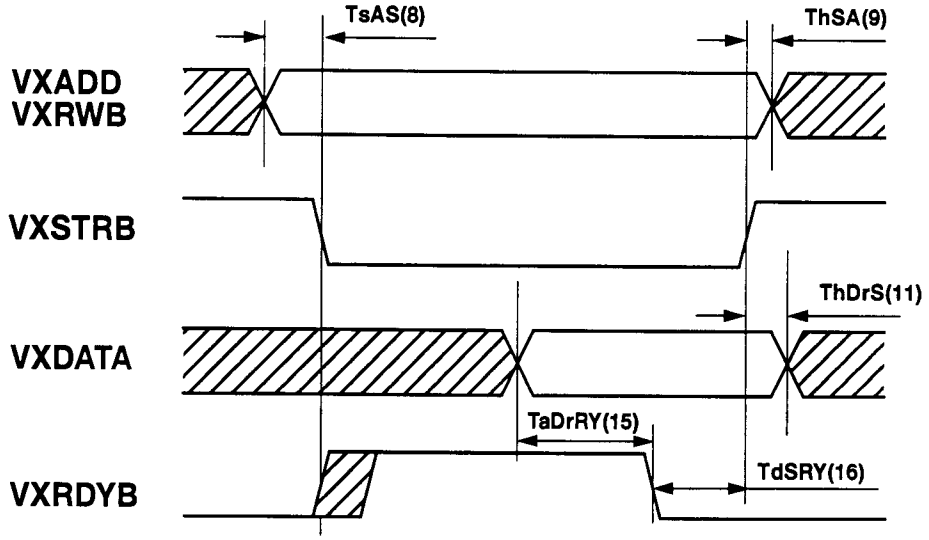
VXDATA Read Cycle



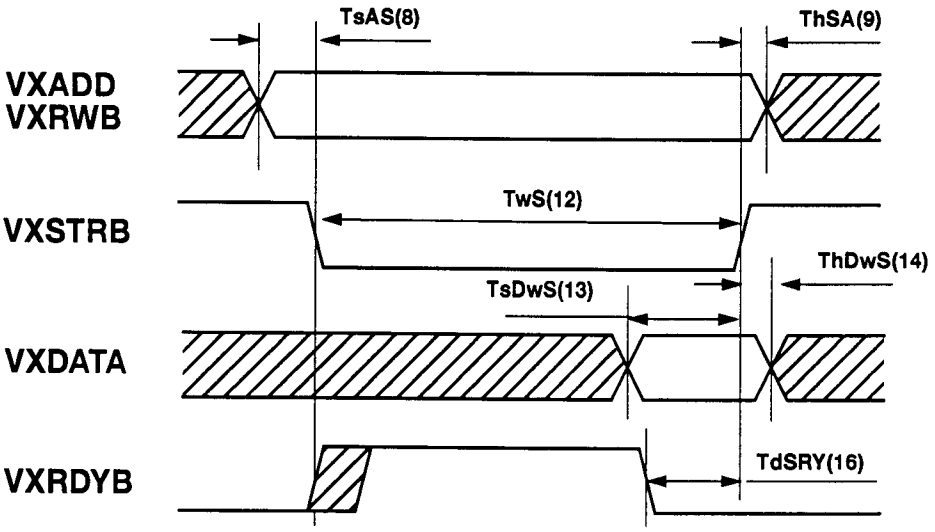
VXDATA Write Cycle

Figure 8. Read/Write Cycle Timings

AC TIMING DIAGRAMS (Continued)



VXDATA Read Cycle with Wait State



VXDATA Write Cycle with Wait State

Figure 9. Read/Write Cycle Timing with Wait State

Pre-Characterization Product:

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com